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DATE: June 13, 2005

CLIENT-MATTER No.: 20880-05093

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U.S. Patent & Trademark Office	703-872-9306	703-308-6673

FROM: Hector J. Ribera

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SENT BY: Dana Chevalier

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NUMBER OF PAGES WITH COVER PAGE: 20 ORIGINAL WILL NOT FOLLOW

## MESSAGE:

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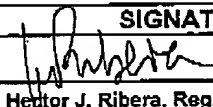
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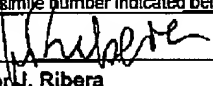
A1000/00103/DOCS/1378903.1

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<b>TRANSMITTAL FORM</b> <i>(to be used for all correspondence during pendency of filed application)</i>	Application Number	09/748,098	
	Filing Date	December 21, 2000	
	First Named Inventor	Nicholas J. Kelsey	
	Group Art Unit Number	2183	
	Examiner Name	Charles A. Harkness	
Total Number of Pages in This Submission	19	Attorney Docket Number	20880-05093

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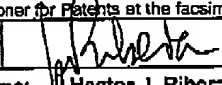
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Attorney/Reg. No.:	Hector J. Ribera, Reg. No. 54,397	Dated: 6/13/2005

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JUN 13 2005

APPLICANTS: Nicholas J. Kelsey, et al.  
SERIAL NO.: 09/748,098  
FILING DATE: December 21, 2000  
TITLE: System and Method for Instruction Level Multithreading in an Embedded Processor Using Zero-Time Context Switching  
EXAMINER: Charles A. Harkness  
GROUP ART UNIT: 2183  
ATTY. DKT. NO.: 20880-05093

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AMENDMENT D AND RESPONSE UNDER 37 C.F.R. §1.116

Sir:

This amendment for the patent application identified above is in response to the Office Action dated April 13, 2005, which set a shortened statutory period for response that expires on July 13, 2005.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 12 of this paper.

Kindly amend this application as indicated herein.